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APPLICATION NO.: 10/666,770

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AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

1        1. (Currently amended) A Boundary-Scan test receiver for capturing  
2 signals during board interconnect testing, comprising:

3            a) a comparator comprising a first input to receive said signals during board  
4 interconnect testing, and a second input to receive a reference voltage, and an output;  
5 and

6            b) a programmable hysteresis circuit coupled to at least one of said comparator  
7 inputs and the output, wherein a portion of the programmable hysteresis circuit  
8 coupled to the output is configured to receive multiple input control signals responsive  
9 to a condition on the board under test.

1        2. (Original) The Boundary-Scan test receiver of claim 1, wherein the  
2 programmable hysteresis circuit comprises a programmable hysteresis voltage  
3 generator.

1        3. (Original) The Boundary-Scan test receiver of claim 2, wherein the  
2 programmable hysteresis voltage generator comprises a current digital-to-analog  
3 converter to sink current from one of the said first and second inputs.

1        4. (Original) The Boundary-Scan test receiver of claim 1, wherein the  
2 programmable hysteresis circuit comprises a programmable hysteresis delay circuit.

1        5. (Original) The Boundary-Scan test receiver of claim 4, wherein the  
2 programmable hysteresis circuit delay circuit comprises a digital-to-analog converter  
3 driving a plurality of variable capacitances, the capacitances being coupled at various  
4 points along a chain of buffer elements.

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1           6. (Original) The Boundary-Scan test receiver of claim 4, wherein the  
2 programmable hysteresis circuit delay circuit comprises a digital-to-analog converter  
3 driving a chain of switchable delay elements.

1           7. (Original) The Boundary-Scan test receiver of claim 1, wherein  
2 programmable inputs of the hysteresis circuit are linked in a scan chain.

1           8. (Currently amended) A Boundary-Scan test receiver for capturing  
2 signals during board interconnect testing, comprising:

3           a) a plurality of comparators, each comprising a first input to receive said  
4 signals during board interconnect testing, and a second input to receive a reference  
5 voltage and an output; and  
6           b) a programmable hysteresis circuit coupled to at least one input and the  
7 output of each comparator, wherein a portion of the programmable hysteresis circuit  
8 coupled to the output is configured to receive multiple input control signals responsive  
9 to a condition on the board under test.

1           9. (Original) The Boundary-Scan test receiver of claim 8, wherein the  
2 programmable hysteresis circuit comprises a programmable hysteresis voltage  
3 generator; the programmable hysteresis voltage generator comprising:

4           a) a voltage divider, coupled between an input of each comparator;  
5           b) a current digital-to-analog converter driving the voltage divider; and  
6           c) a current mirror, coupled to a midpoint of the voltage divider to mirror a  
7 reference voltage at said midpoint.

1           10. (Original) The Boundary-Scan test receiver of claim 8, wherein the  
2 programmable hysteresis circuit comprises a programmable hysteresis voltage  
3 generator; the programmable hysteresis voltage generator comprising:  
4           a) a voltage divider, coupled between an input of each comparator;  
5           b) a current digital-to-analog converter driving the voltage divider; and  
6           c) a current mirror, coupled to a midpoint of the voltage divider to mirror a  
7 common mode voltage of said signals at said midpoint.

1           11. (Currently amended) A Boundary-Scan test method, comprising:  
2           a) determining at least one operating condition of a board under test;  
3           b) in response to said determined at least one operating condition,  
4           programming hysteresis circuits of Boundary-Scan test receivers in the board under  
5           test, wherein programming comprises the application of at least one of a data input  
6           signal, a first control signal that determines an active path through the programmable  
7           hysteresis circuit, a second control signal that directs operation of a data capture  
8           device, and a third control signal that directs operation of an update device; and  
9           c) executing a Boundary-Scan test.

1           12. (Original) The BoundarScan test method of claim 11, wherein  
2           determining the at least one operating condition comprises determining a signaling  
3           level of a component of the board under test.

1           13. (Original) The Boundary-Scan test method of claim 11, wherein  
2           determining the at least one operating condition comprises determining a noise level  
3           associated with signal paths of the board under test.

1           14. (Original) The Boundary-Scan test method of claim 13, further  
2           comprising, prior to determining the at least one operating condition:  
3           a) programming hysteresis circuits of the Boundary-Scan test receivers with  
4           default values; and  
5           b) executing a Boundary-Scan test; wherein determining the noise level  
6           associated with signal paths of the board under test comprises evaluating results of the  
7           Boundary-Scan test ran with the default values.

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1           15. (Original) The Boundary-Scan test method of claim 11, further  
2 comprising, prior to determining the at least one operating condition:

3           a) programming hysteresis circuits of the Boundary-Scan test receivers with  
4 default values; and

5           b) executing a Boundary-Scan test; wherein determining the at least one  
6 operating condition of the board under test comprises evaluating results of the  
7 Boundary-Scan test ran with the default values.

1           16. (Original) The Boundary-Scan test method of claim 11, wherein  
2 programming the hysteresis circuits comprises programming a hysteresis voltage.

1           17. (Original) The Boundary-Scan test method of claim 11, wherein  
2 programming the hysteresis circuits comprises programming a hysteresis delay.

1           18. (Original) The Boundary-Scan test method of claim 11, wherein  
2 the hysteresis circuits of a component of a board under test are programmed via bits  
3 shifted through a scan chain.

1           19. (Original) The Boundary-Scan test method of claim 11, wherein  
2 the hysteresis circuits of a component of a board under test are programmed in a  
3 plurality of sets.

1           20. (New)         The Boundary-Scan test receiver of claim 1, wherein the  
2 programmable hysteresis circuit receives a data input signal, a first control signal that  
3 determines an active path through the programmable hysteresis circuit, a second  
4 control signal that directs operation of a data capture device, and a third control signal  
5 that directs operation of an update device.